GL4H-QDSM31FR4C

QSFP-DD 400Gb/s 1310nm 2km LC Transceiver

PRODUCT FEATURES

- Up to 2km transmission on single mode fiber (SMF) with FEC
- Compliant with CMIS4.0 Management interface specifications
- Compliant with 400G-FR4 optical specifications
- 4 CWDM lanes MUX/DEMUX design
- Compliant to QSFP-DD MSA
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Single +3.3V power supply
- Case temperature range: 0 ~ +70°C
- Maximum power consumption 10W
- Duplex LC connector
- RoHS complaint

APPLICATIONS

- Data Center Interconnect
- 400G Ethernet
- Infiniband Interconnect
- Enterprise Networking

PRODUCT DESCRIPTION

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2 km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion

in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Table1. Ordering information

Product part Number	Date Rate (Gbps)	Media	Wavelength (nm)	Transmission Distance	Temperature Range （Tcase）（℃）	
GL4H-QDSM31FR4C	400	SMF	1271nm 1291nm 1311nm 1331nm	2km	0~70	Commercial

Table2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	10	90	%
Supply Voltage	Vcc	0	4	V

Table3. Recommended Operating Conditions

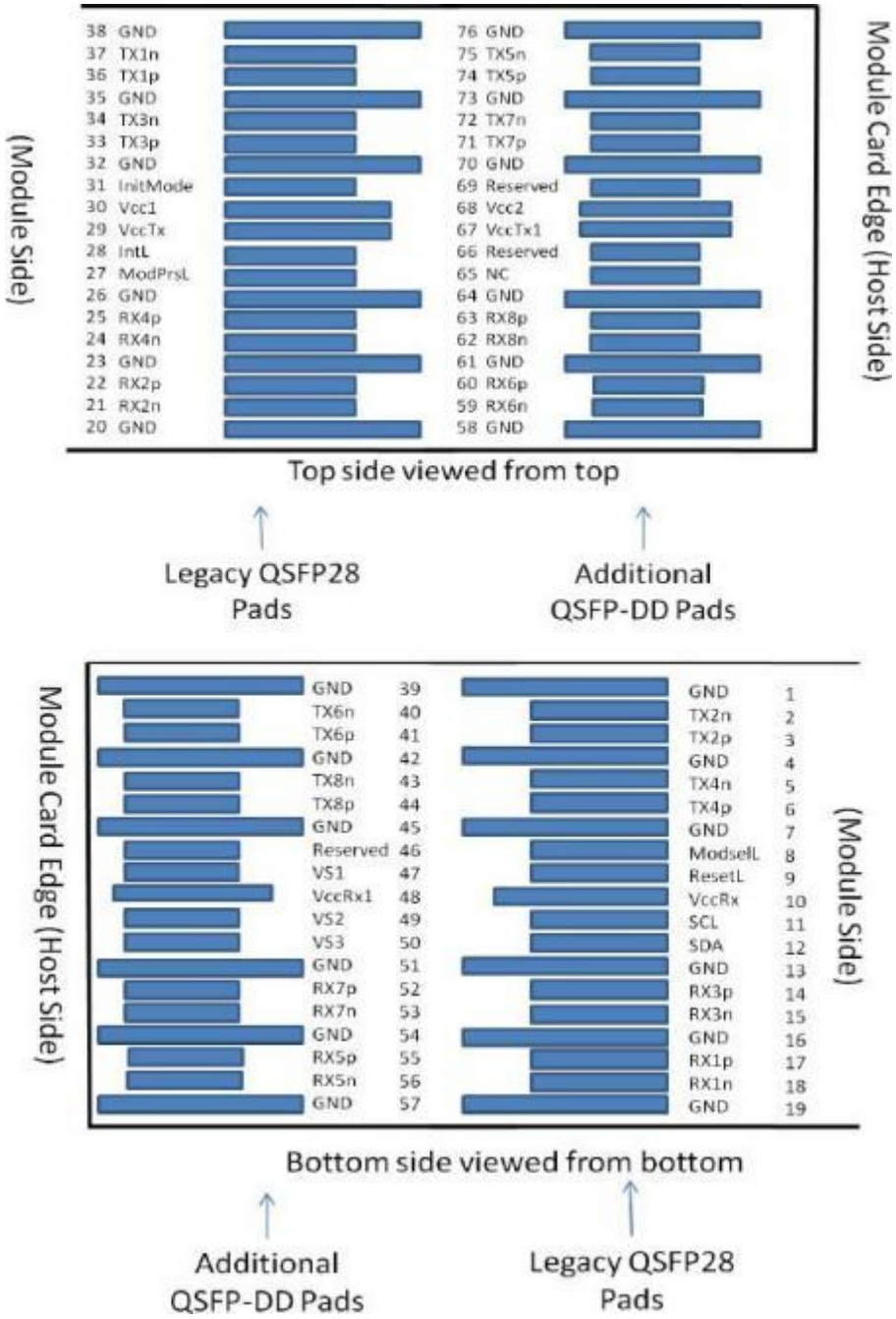
Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Supply Voltage	Vcc	3.14	3.3	3.46	V
Pre-FEC BER				2.4×10^{-4}	
Power Consumption	P_{Diss}			10	W
Link Distance		2		2000	m

Table4. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Modulation Format			PAM4			
Data Rate, each lane			53.125±100 ppm		GBd	
Side-mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			9.3	dBm	
Average Launch Power, each lane	P_{AVG}	-3.3		3.5	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	P_{OMA}	-0.3		3.7	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lane for ER ≥ 4.5dB for ER < 4.5dB		 -1.7 -1.6			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
TDECQ – $10*\log_{10}$(Ceq), each Lane				3.4	dB	3
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	dB	
$RIN_{21.4}OMA$	RIN			-136	dB/HZ	

Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-20	dBm	
Receiver						
Modulation Format			PAM4			
Data Rate, each lane			53.125±100 ppm		GBd	
Damage Threshold, each Lane	TH_d	4.5			dBm	4
Average Receive Power, each Lane		-7.3		3.5	dBm	5
Receive Power (OMA_{outer}), each Lane				3.7	dB	
Difference in Launch Power between any Two Lanes(OMA_{outer})				4.1	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation (1)	dBm	6
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-2.6	dBm	7
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-20			dBm	
LOS De-assert	LOSD			-10.3	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Pin Description



QSFP-DD compliant 76 pin connector

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1

2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2

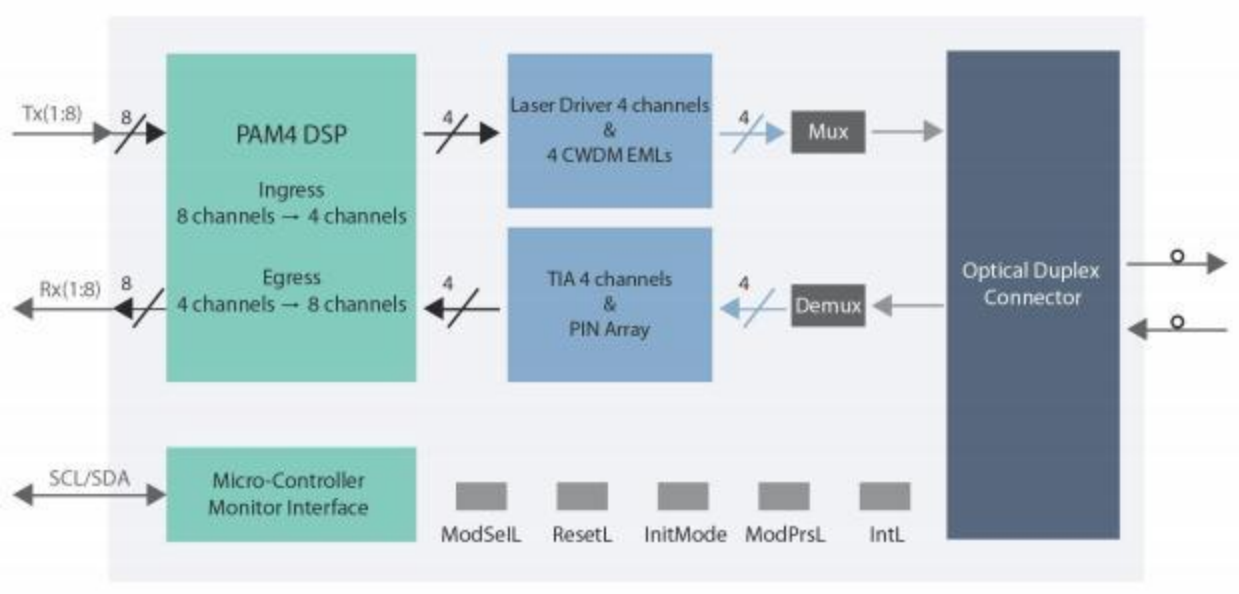
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reseved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reseved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76		GND	Ground	1A	1

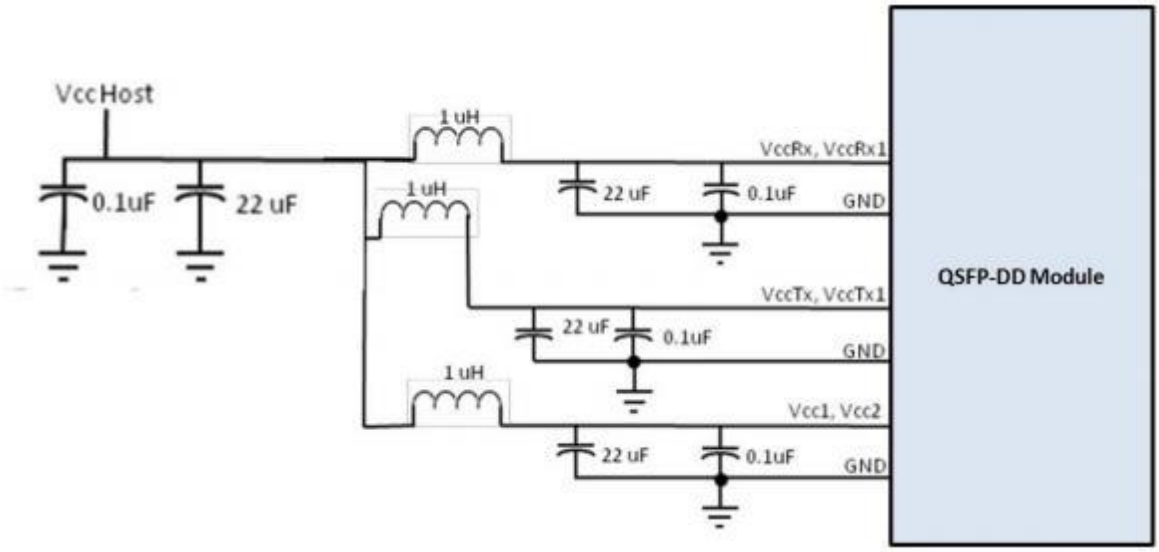
Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 Kohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

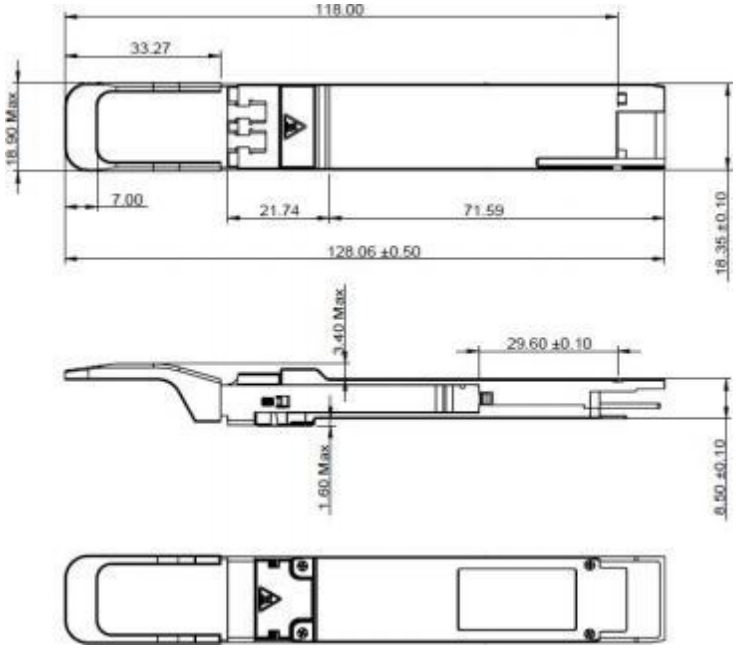
Module Block Diagram



Recommended Power Supply Filter



Mechanical Dimensions



Regulatory Compliance

Agency	Standard	Certificate /Comments
CE-EMC	EN 55032: 2015	17706703 003
	EN 55024: 2010+A1	
REACH	REACH SVHC 197	68.420.19.0344.01
FCC	FCC Rules and Regulations Part 15 Subpart B Class B	MTi190422E141C
RoHS	2011/65/EU and amendment (EU) 2015/863	68.420.17.1030.01