GL4H-QDSM31DR4C

QSFP-DD 400Gb/s 1310nm 500m MPO Transceiver

PRODUCT FEATURES

- Up to 500m transmission on single mode fiber (SMF) with FEC
- Compliant with CMIS4.0 Management interface specifications
- Compliant with 400G-DR4 optical specifications
- Four Parallel 1310nm Optical Lanes
- Compliant to QSFP-DD MSA
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 10W
- MPO-12 Connector
- RoHS complaint

APPLICATIONS

- Data Center Interconnect
- 400G Ethernet
- Infiniband Interconnect

PRODUCT DESCRIPTION

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 500m optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of 1310 optical signals. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Table1. Ordering information

Product part Number	Date Rate (Gbps)	Media	Wavelength (nm)	Transmission Distance	Temperature Range （Tcase）（℃）	
GL4H-QDSM31DR4C	400	SMF	1310	500m	0~70	Commercial

Table2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	10	90	%
Supply Voltage	Vcc	0	4	V

Table3. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Supply Voltage	Vcc	3.14	3.3	3.46	V
Pre-FEC BER				2.4×10^{-4}	
Power Consumption	P_{Diss}			10	W
Link Distance		2		2000	m

Table4. Optical Characteristics

Parameter	Unit	Min	Typ.	Max	Note
Transmitter					
Signaling rate, each lane	GBd		53.125 ± 100 ppm		PAM4
TX Central Wavelength	nm	1304.5	1310	1317.5	
Side-mode Suppression Ratio (SMSR)	dB	30			
Average Launch Power, each lane	dBm	-2.9		4	1
Outer Optical Modulation Amplitude (OMAouter), each lane	dBm	-0.8		4.2	2

Parameter	Unit	Min	Typ.	Max	Note
Launch Power in OMAouter minus TDECQ, each Lane(min)	dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane (max)	dB			3.4	3
Average Launch Power of OFF Transmitter, each lane (max)	dBm			-15	
Extinction Ratio, each lane (min)	dB	3.5			
Optical Return Loss Tolerance (max)	dB			21.4	
RIN21.4OMA (max)	dB/Hz			-136	
Transmitter Reflectance (max)	dB			-26	

Receiver

| Parameter	Unit	Min	Typ.	Max	Note
Signaling Rate, each lane	Gbps		53.125 $\pm$ 100 ppm		PAM4
RX Central Wavelength	nm	1304.5	1310	1317.5	
Damage Threshold (min)	dBm	5			4
Average Receive Power per Lane	dBm	-5.9		4.0	5
Receiving Power (OMAouter) per Lane	dBm			4.2	
Receiver Reflectance (max)	dB			-26	
Receiver Sensitivity (OMAouter), each lane (max)	dBm		Equation (1)		6
Stressed Receiver Sensitivity (OMAouter) per Lane	dBm			-1.9	7

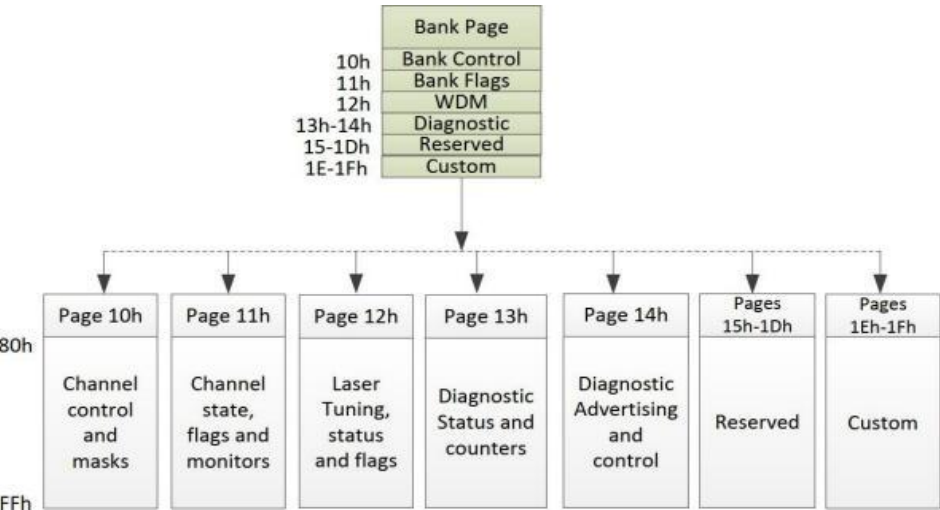| Parameter	Unit	Min.	Typ.	Max.	Note
Conditions of Stressed Receiver Sensitivity Test					
Stressed Eye Closure for PAM4 (SECQ), lane under test	dB		3.4		8
OMAouter of each aggressor lane	dBm			4.2	
LOS Assert	dBm	-15			
LOS De-Assert	dBm			-8.9	
LOS Hysteresis	dB	0.5			

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance;

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMAouter (min) must exceed the minimum value specified here;

3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement;

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance;

5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power;

6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: RS=max (−3.9, SECQ−5.3), where RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity. which is illustrated in the Figure;
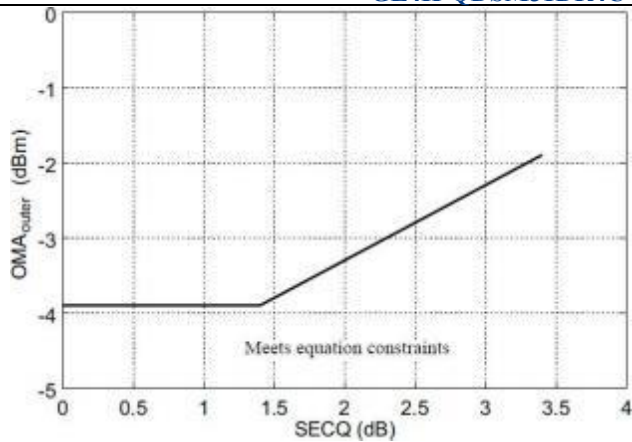
7. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4;

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

Parameter	Unit	Error	Note
Temperature Monitor	℃	±3	1LSB= 1/256℃
Supply Voltage Monitor	V	±0.1	1LSB= 100 uV
Bias Current Monitor	mA	± 10%	1 LSB= 2 uA
TX Power Monitor	dBm	±3	1LSB=0. 1uW
RX Power Monitor	dBm	±3	1LSB=0. 1uW

Pin Description

Top side viewed from top

Legacy QSFP28 Pads   Additional QSFP-DD Pads

Bottom side viewed from bottom

Additional QSFP-DD Pads   Legacy QSFP28 Pads
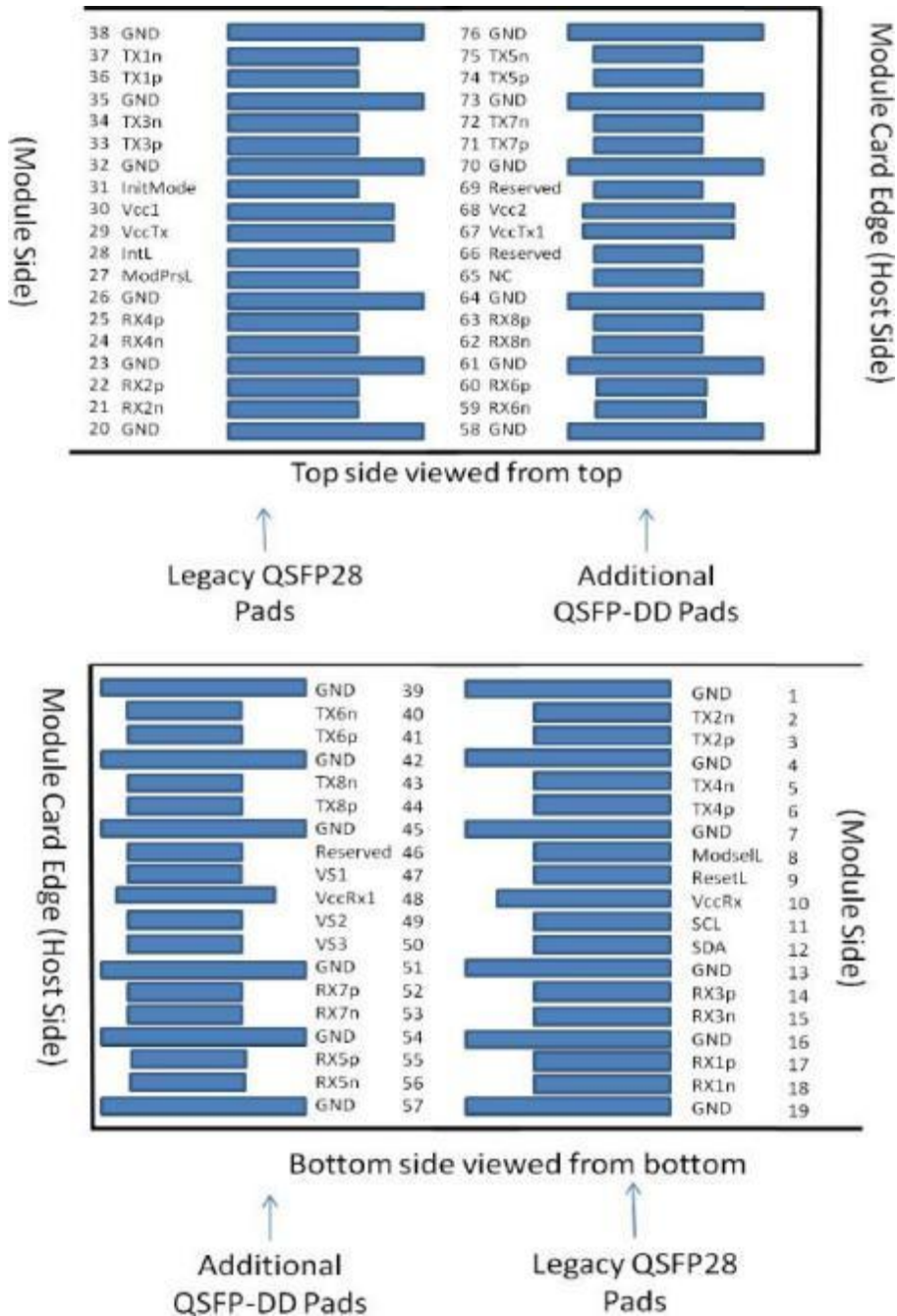
QSFP-DD compliant 76 pin connector

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	

3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

| 26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2

49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reseved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reseved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 Kohms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

ecommended Power Supply Filter

Mechanical Dimensions

Optical Interface
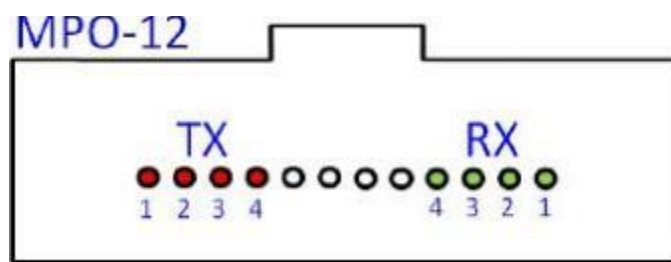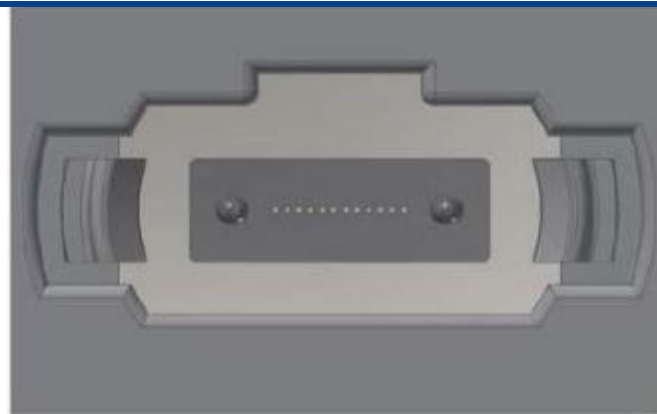
Regulatory Compliance

Agency	Standard	Certificate /Comments
CE-EMC	EN 55032: 2015	17706703 003
	EN 55024: 2010+A1	
REACH	REACH SVHC 197	68.420.19.0344.01
FCC	FCC Rules and Regulations Part 15 Subpart B Class B	MTi190422E141C
RoHS	2011/65/EU and amendment (EU) 2015/863	68.420.17.1030.01